

**IN THE CLAIMS**

Claims 1-48 (cancelled)

49. (New) A processing device comprising:

a reconfigurable circuit consisted of  $N$  stages, where  $N > 1$ , each of the stages having a plurality of arithmetic logic units,

an internal state holding circuit located between the stages, and

a control portion controlling setting data so that setting data A and B are successively supplied to the reconfigurable circuit to configure an intended circuit, the data A and B being divided to units A1, A2, .... and B1, B2, ..., respectively; wherein

when the unit A1 is set to an  $M$ th stage at one time point, where  $N > M > 1$ ,

the control portion sets the unit A2 to a  $(M+1)$ th stage, sets the unit B1 to the  $M$ th stage, and sets output data of the unit A1 to the  $(M+1)$ th stage at a next time point, and

when the unit A1 is set to an  $N$ th stage at one time point,

the control portion sets the unit A2 to the first stage, sets the unit B1 to the  $N$ th stage, and sets the output data of the unit A1 to the first stage.